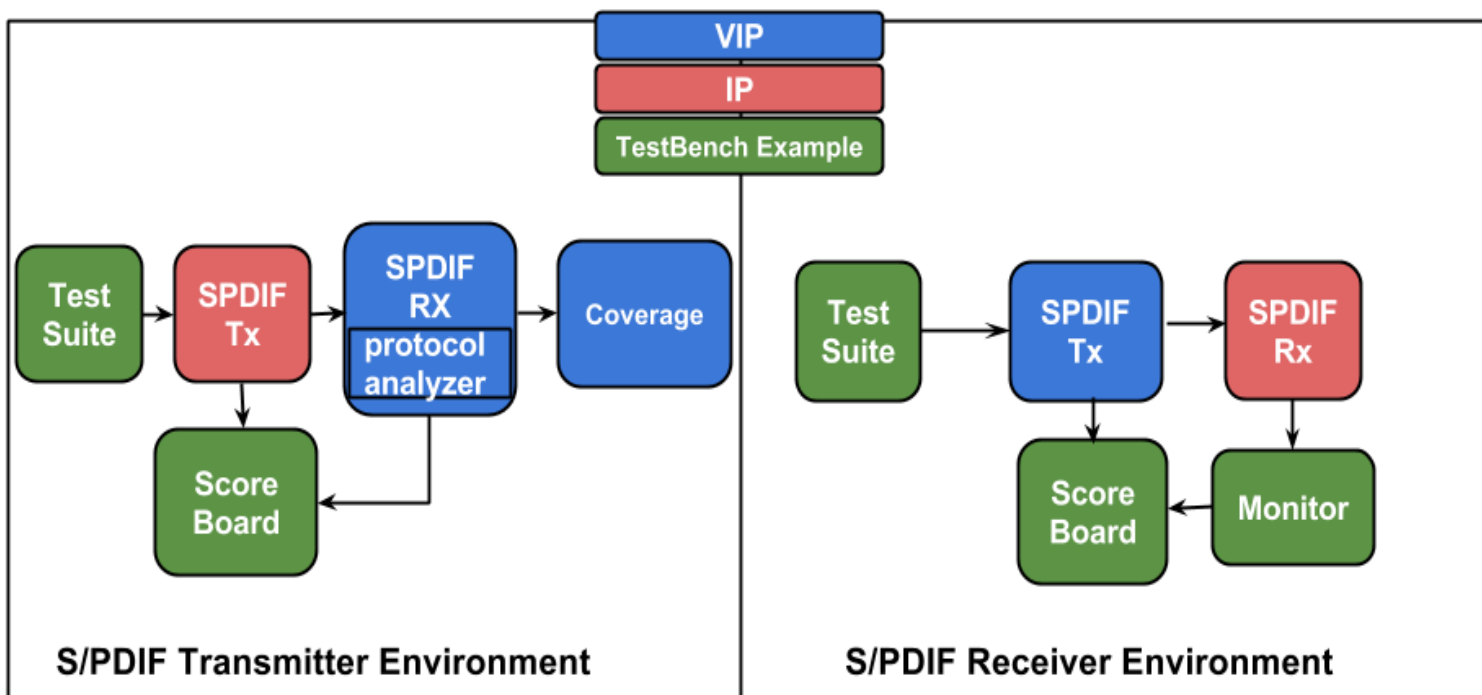


S/PDIF Tx/Rx VIP

Boost Valley offers the S/PDIF Verification IP as part of its InspiringVIP product line. The S/PDIF VIP is highly flexible and configurable. It can act as a Transmitter or Receiver. It can also act as a protocol analyzer. The VIP is written in SystemVerilog and can be inside any verification environment based on UVM.

The VIP comes along with a comprehensive user's manual, a set of test examples and an RTL Verilog S/PDIF Transmitter/Receiver DUT. VIP customizations can be developed on-demand.



Overview

- VIP: S/PDIF VIP.
- Compliance: IEC 60958 Standard
- Language: SystemVerilog.
- Methodology : UVM v1.1d/UVM 1.2
- Simulators: QuestaSim, VCS

Features

- Compliant functionality with IEC 60958 specification
- Supports both Transmitter and Receiver
- Configurable Baud rate
- Configurable Transaction Depth
- Bi-Phase Mark - BMC encoding
- Preamble Error injection
- Parity Error Injection
- Constrained randomized frames

Deliverables

- Test-cases to test all supported S/PDIF features.
- Built-in coverage analysis model.
- VIP User's Manual.
- S/PDIF UVM Verification IP.
- Sample ScoreBoard.
- S/PDIF DUT RTL Code. **{Extra}**

VIP Configurations

- Baud rate
- Transaction Depth

Other VIPs

- HDMI 1.4/2.0 VIP
- I2S VIP
- I2C Master / Slave VIP
- MIPI CPHY VIP
- UART VIP
- SPI VIP
- Coming Soon:
 - V-by-One VIP
 - MIPI DPHY VIP

About Boost Valley

Boost Valley is a digital design and verification specialized firm, building its own portfolio of Verification IPs as well as providing clients with Senior level quality consultation services in Digital Design/Verification domains. Our goal is to establish strategic alliances designed to help deliver a client-centric, total solutions approach for solving problems, exploiting business opportunities and creating sustainable competitive advantage for our clients.

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